ABSTRACT OF THE DISCLOSURE

[1030] A mechanism has been developed by which the impact on speed from back end-of-line interconnect layers may be characterized. A method for designing interconnect layers of an integrated circuit includes coupling a capacitive load to a speed sensing circuit to measure a delay corresponding to an interconnect structure of an integrated circuit design, selectively configuring the capacitive load by selectively coupling at least one of a plurality of capacitive structures, the capacitive structures including at least a portion of a plurality of metal layers. The capacitive load is representative of the interconnect structure. The method includes measuring the delay corresponding to the capacitive load to characterize at least one layer of the interconnect structure. In some realizations, the method also includes characterizing the interconnect structure based at least in part on the delay measurement.